Amendment in the Claims

Claims 1-57 (cancelled).

58. (Currently Amended) A processor, comprising:

a Boolean logic circuit, wherein the Boolean logic circuit is operated for performing the short-circuit evaluation of Normal Form Boolean expressions/operations;

a plurality of input/output interface circuits coupled to the Boolean logic circuit, wherein the plurality of input/output interface circuits are operated for receiving a plurality of compiled Boolean expressions/operations and transmitting a plurality of compiled results; and

a plurality of multi-bit registers coupled to the plurality of input/output interface circuits, wherein the plurality of multi-bit registers comprise an instruction register, a first address register and a second address register,

wherein if the Boolean logic circuit is operated for performing the short-circuit evaluation of Conjunctive Normal Form ("CNF") Boolean expressions/operations, then the first address register is activated as a next operation address register and the second address register is activated as an end of OR address register, the output of the first address register is an address of a CNF expression immediately following the CNF expression being evaluated, and the output of the second address register is the address of the conjunct immediately following the conjunct being evaluated, wherein the output occurs in the event that the Boolean logic unit delivers an indication that the final evaluation of the CNF expression has been determined (false) to the first address register or an indication that the final evaluation of the current conjunct has been determined (true) to the second address register,

wherein if the Boolean logic circuit is operable for performing the short-circuit evaluation of Disjunctive Normal Form ("DNF") Boolean expressions/operations, then the first address register is activated as an end of operation address register and the second address register is activated as an end of AND address register, the output of the first address register is the address of the DNF expression immediately following the DNF expression being evaluated and the output of the second address register is the address of the disjunct immediately following the disjunct being evaluated, wherein the output occurs in the event that the Boolean logic unit delivers an indication that the final evaluation of the DNF expression has been determined (true)

to the first address register or an indication that the final evaluation of the current disjunct has been determined (false) to the second address register, and

wherein if the Boolean logic circuit is operated for performing the short-circuit evaluation of both Conjunctive and Disjunctive Normal Form Boolean expressions/operations, then the first address register is activated as a next operation/end of operation address register and the second address register is activated as an end of OR/AND address register, the output of the first address register is the address of the CNF/DNF expression immediately following the current CNF/DNF expression and the output of the second address register is the address of the conjunct/disjunct immediately following the current conjunct/disjunct, wherein the output occurs in the event that the Boolean logic unit delivers an indication that the final evaluation of the CNF/DNF expression has been determined to the first address register or an indication that the final evaluation of the current conjunct/disjunct has been determined to the second address register.

59. (Original) The processor of claim 58, wherein the instruction register comprises a register that is n+m+x bits wide and includes an n-bit address, an m-bit control/state word, and an x-bit operational code.

60. (Original) The processor of claim 59, wherein the instruction register comprises a register that is n+m+3 bits wide and includes an operational code that is 3 bits wide.

61. (Original) The processor of claim 59, wherein the operational code is more than 3 bits wide.

62. (Previously Presented) The processor of claim 59, wherein the first and second address registers are n+m bits wide, and wherein the Boolean logic circuit is operable to load both the n-bit address and the m-bit wide control/state word from the instruction register into the first and second address registers to form an address that is n+m bits wide.

63. (Previously Presented) The processor of claim 59, wherein the Boolean logic circuit is operable to associate each of a plurality of logical addresses with a respective physical address in a control store, and operated to retrieve a particular physical address from the control store based on the associated logical address present in one of the first or second address registers.

64. (Original) The processor of claim 58, wherein the first address register stores an address used for Boolean short-circuiting.

65. (Original) The processor of claim 58, wherein the second address register stores the address of an instruction immediately following a conjunct comprising an OR clause, or the address of an instruction immediately following a disjunct comprising an AND clause.

Claims 66-102 (cancelled).

103. (Currently Amended) A computing device, comprising: a general-purpose processor; and a Boolean co-processor that accepts code, representative of Boolean code, from the general-purpose processor, the Boolean processor including:

a Boolean logic circuit, wherein the Boolean logic circuit is operated for performing the short-circuit evaluation of Conjunctive Normal Form Boolean expressions/operations, operated for performing the short-circuit evaluation of Disjunctive Normal Form Boolean expressions/operations, or operated for performing the short-circuit evaluation of both Conjunctive Normal Form Boolean expressions/operations and Disjunctive Normal Form Boolean expressions/operations;

a plurality of input/output interface circuits coupled to the Boolean logic circuit, wherein the plurality of input/output interface circuits are operated for receiving a plurality of compiled Boolean expressions/operations and transmitting a plurality of compiled results; and

a plurality of multi-bit registers coupled to the plurality of input/output interface circuits, wherein the plurality of multi-bit registers comprise an instruction register, a first address register and a second address register,

wherein if the Boolean logic circuit is operated for performing the short-circuit evaluation of Conjunctive Normal Form ("CNF") Boolean expressions/operations, then the first address register is selected as a next operation address register and the second address register is selected as an end of OR address register, the output of the first address register is an address of a CNF expression immediately following the CNF expression being evaluated, and the output of the second address register is the address of the conjunct immediately following the conjunct being

evaluated, wherein the output occurs in the event that the Boolean logic unit delivers an indication that the final evaluation of the CNF expression has been determined (false) to the first address register or an indication that the final evaluation of the current conjunct has been determined (true) to the second address register,

wherein if the Boolean logic circuit is operated for performing the short-circuit evaluation of Disjunctive Normal Form ("DNF") Boolean expressions/operations, then the first address register is selected as an end of operation address register and the second address register is selected as an end of AND address register, the output of the first address register is the address of the DNF expression immediately following the DNF expression being evaluated and the output of the second address register is the address of the disjunct immediately following the disjunct being evaluated, wherein the output occurs in the event that the Boolean logic unit delivers an indication that the final evaluation of the DNF expression has been determined (true) to the first address register or an indication that the final evaluation of the current disjunct has been determined (false) to the second address register, and

wherein if the Boolean logic circuit is operated for performing the short-circuit evaluation of both Conjunctive and Disjunctive Normal Form Boolean expressions/operations, then the first address register is selected as a next operation/end of operation address register and the second address register is selected as an end of OR/AND address register, the output of the first address register is the address of the CNF/DNF expression immediately following the current CNF/DNF expression and the output of the second address register is the address of the conjunct/disjunct immediately following the current conjunct/disjunct, wherein the output occurs in the event that the Boolean logic unit delivers an indication that the final evaluation of the CNF/DNF expression has been determined to the first address register or an indication that the final evaluation of the current conjunct/disjunct has been determined to the second address register.

104. (Original) The computing device of claim 103, wherein the instruction register comprises a register that is n+m+x bits wide and includes an n-bit address, an m-bit control/state word, and an x-bit operational code.

105. (Original) The computing device of claim 103, wherein the first address register stores an address used for Boolean short-circuiting.

106. (Original) The computing device of claim 103, wherein when evaluating Conjunctive Normal Form Boolean expressions/operations, the second address register stores the address of an instruction immediately following a conjunct comprising an OR clause, and when evaluating Disjunctive Normal Form Boolean expressions/operations, the second address register stores the address of an instruction immediately following a disjunct comprising an AND clause.

107. (Original) The computing device of claim 106, wherein the instruction whose address is stored in the second address register is another conjunct or disjunct, respectively.

Claims 108-126 (cancelled).

127. (Currently Amended) A hybrid processor, comprising: a host processor, wherein the host processor is at least operated for performing comparison operations and register modifications; and a Boolean processor core, comprising:

a Boolean short-circuit outcome calculation circuit, wherein the Boolean short-circuit outcome calculation circuit is operated for evaluating the short-circuit outcome of Conjunctive Normal Form Boolean expressions/operations, operated for evaluating the short-circuit outcome of Disjunctive Normal Form Boolean expressions/operations, or operated for evaluating the short-circuit outcome of both Conjunctive Normal Form Boolean expressions/operations and Disjunctive Normal Form Boolean expressions/operations;

a plurality of input/output interface circuits coupled to the Boolean [[c]]short-circuit outcome calculation circuit, wherein the plurality of input/output interface circuits are operated for receiving, from the host processor, data related to a plurality of compiled Boolean expressions/operations and transmitting, to the host processor, data representative of the short-circuit outcome of a plurality of evaluated Normal Form Boolean expressions/operations; and

a plurality of multi-bit registers coupled to the plurality of input/output interface circuits, wherein the plurality of multi-bit registers comprise a first address register and a second address register,

wherein if the Boolean short-circuit outcome calculation circuit is operated for evaluating the short-circuit outcome of Conjunctive Normal Form ("CNF") Boolean expressions/operations,

then the first address register is selected as a next operation address register and the second address register is selected as an end of OR address register, the output of the first address register is an address of a CNF expression immediately following the CNF expression being evaluated, and the output of the second address register is the address of the conjunct immediately following the conjunct being evaluated, wherein the output occurs in the event that the Boolean logic unit delivers an indication that the final evaluation of the CNF expression has been determined (false) to the first address register or an indication that the final evaluation of the current conjunct has been determined (true) to the second address register,

wherein if the Boolean short-circuit outcome calculation circuit is operated for evaluating the short-circuit outcome of Disjunctive Normal Form ("DNF") Boolean expressions/operations, then the first address register is selected as an end of operation address register and the second address register is an end of AND address register, the output of the first address register is the address of the DNF expression immediately following the DNF expression being evaluated and the output of the second address register is the address of the disjunct immediately following the disjunct being evaluated, wherein the output occurs in the event that the Boolean logic unit delivers an indication that the final evaluation of the DNF expression has been determined (true) to the first address register or an indication that the final evaluation of the current disjunct has been determined (false) to the second address register, and

wherein if the Boolean short-circuit outcome calculation circuit is operated for evaluating the short-circuit outcome of both Conjunctive and Disjunctive Normal Form Boolean expressions/operations, then the first address register is selected as a next operation/end of operation address register and the second address register is selected as an end of OR/AND address register, the output of the first address register is the address of the CNF/DNF expression immediately following the current CNF/DNF expression and the output of the second address register is the address of the conjunct/disjunct immediately following the current conjunct/disjunct, wherein the output occurs in the event that the Boolean logic unit delivers an indication that the final evaluation of the CNF/DNF expression has been determined to the first address register or an indication that the final evaluation of the current conjunct/disjunct has been determined to the second address register.

128. (Original) The hybrid processor of claim 127, wherein the first register stores an

address used by the host processor for Boolean short-circuiting.

129. (Original) The hybrid processor of claim 127, wherein when evaluating Conjunctive Normal Form Boolean expressions/operations, the second address register stores the address of an instruction immediately following a conjunct comprising an OR clause, and when evaluating Disjunctive Normal Form Boolean expressions/operations, the second address register stores the address of an instruction immediately following a disjunct comprising an AND clause.

130. (Original) The hybrid processor of claim 127, wherein at least one of the first and second address registers stores an address that is transmitted to the host processor by the plurality of input/output interfaces as the short-circuit outcome of a plurality of evaluated Normal Form Boolean expressions/operations.

131. (Original) The hybrid processor of claim 130, wherein the address is transmitted to a memory device in the host processor.

132. (Original) The hybrid processor of claim 131, wherein the address is transmitted to a register in the host processor.

133. (Original) The hybrid processor of claim 131, wherein the address is transmitted to a program counter in the host processor.

134. (Original) The hybrid processor of claim 127, wherein loading the first address register activates the Boolean processor core.

135. (Original) The hybrid processor of claim 127, wherein a predetermined input from the host processor deactivates the Boolean processor core, thereby preventing the Boolean processor core from transmitting, to the host processor, any short-circuit outcome data.

136. (Original) The hybrid processor of claim 127, wherein a predetermined input from

the host processor resets an OR conjunct and/or AND disjunct register, thereby notifying the Boolean processor core than an OR conjunct or AND disjunct has ended.

Claims 137-146 (cancelled).

147. (New) A processor, comprising:

a Boolean logic circuit, wherein the Boolean logic circuit is operated for performing the short-circuit evaluation of Normal Form Boolean expressions/operations;

a plurality of input/output interface circuits coupled to the Boolean logic circuit, wherein the plurality of input/output interface circuits are operated for receiving a plurality of compiled Boolean expressions/operations and transmitting a plurality of compiled results; and

a plurality of multi-bit registers coupled to the plurality of input/output interface circuits, wherein the plurality of multi-bit registers comprise an instruction register, a first address register and a second address register,

wherein if the Boolean logic circuit is operated for performing the short-circuit evaluation of Conjunctive Normal Form ("CNF") Boolean expressions/operations, then the first address register is activated as a next operation address register and the second address register is activated as an end of OR address register, wherein the first address register outputs an address of a next CNF expression if the final evaluation of the CNF expression has been determined to be false, and wherein the second address register outputs a next conjunct if the final evaluation of a current conjunct has been determined to be true,

wherein if the Boolean logic circuit is operable for performing the short-circuit evaluation of Disjunctive Normal Form ("DNF") Boolean expressions/operations, then the first address register is activated as an end of operation address register and the second address register is activated as an end of AND address register, wherein the first address register outputs an address of a next DNF expression if the final evaluation of the DNF expression has been determined to be true, and wherein the second address register outputs a next disjunct if the final evaluation of a current disjunct has been determined to be false, and

wherein if the Boolean logic circuit is operated for performing the short-circuit evaluation of both Conjunctive and Disjunctive Normal Form Boolean expressions/operations, then the first address register is activated as a next operation/end of operation address register and the second

address register is activated as an end of OR/AND address register, wherein the first address register outputs an address of a next CNF/DNF expression if the final evaluation of the CNF/DNF expression has been determined, and wherein the second address register outputs a next conjunct/disjunct if the final evaluation of a current conjunct/disjunct has been determined.

148. (New) The processor of claim 147, wherein the instruction register comprises a register that is n+m+x bits wide and includes an n-bit address, an m-bit control/state word, and an x-bit operational code.

149. (New) The processor of claim 147, wherein the instruction register comprises a register that is n+m+3 bits wide and includes an operational code that is 3 bits wide.

150. (New) The processor of claim 147, wherein the first address register stores an address used for Boolean short-circuiting.